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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/375,328	08/17/1999	AHMAD R. ANSARI	M-7669-US	4890
33031	7590	07/02/2004	EXAMINER	
CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			ELLIS, RICHARD L	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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**Advisory Action**

Application No.

09/375,328

Applicant(s)

ANSARI, AHMAD R.

Examiner

Richard Ellis

Art Unit

2183

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 03 June 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY** [check either a) or b)]

- a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.  
2. ☒ The proposed amendment(s) will not be entered because:  
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ they raise the issue of new matter (see Note below);  
(c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: The submitted amendment made no changes to the claim language.

3. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
4. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.  
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.  
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☒ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:


Claim(s) allowed: None.

Claim(s) objected to: None.

Claim(s) rejected: 53-54, 56-66, 69-78, 80-88.

Claim(s) withdrawn from consideration: \_\_\_\_\_.

8. ☐ The drawing correction filed on \_\_\_\_\_ is a) ☐ approved or b) ☐ disapproved by the Examiner.  
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_.  
10. ☐ Other: \_\_\_\_\_

  
RICHARD L. ELLIS  
PRIMARY EXAMINER

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Continuation of 5. does NOT place the application in condition for allowance because: Applicant argues that Birritella does not teach "generating a vector transfer unit exception if a second program attempts to transfer data ..." because applicant asserts that Birritella "teaches that instructions, not programs, can attempt to access a vector buffer."

Initially, it is noted that applicant's own specification indicates that in applicant's own invention, it is "instructions", not "programs" which access the vector buffer (pg. 24, lines 5-6, "the current program can access the active vector buffer in VBP 208 through VTU instructions."

Secondly, it is noted that programs consist of instructions, so that existence of instructions indicates existence of programs. Therefore, by teaching that a second instruction is prevented from accessing a buffer in use by a first instruction, Birritella is also teaching preventing access by first and second programs containing those first and second instructions.

Additionally, applicant argues regarding Birritella that "Birritella teaches a system that 'stalls all instructions currently executing' if a second instruction attempts to access a vector buffer while an indicator is in the live state". It is pointed out that if Birritella functions as argued by applicant, that blocking access by a second instruction in a same program by "stall[ing] all instructions currently executing" would result in a dead-lock situation where the processor would grind to a complete halt. Therefore, the only way that "stall[ing] all instructions currently executing" would produce a working system is if the intended meaning is "stalling all instructions in a second program when that second program attempts to access the vector buffer."

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